

identified patent application, please enter this Response and consider the following:

REMARKS

I. Status of the Application

Claims 1-12 are pending in this application. In the December 30, 2002 Office Action, the Examiner:

- A. Objected to the Drawings;
- B. Objected to Claims 5 and 11;
- C. Rejected claims 1-12 under 35 U.S.C. §112, first paragraph;
- D. Rejected claims 1-6 and 8-12 under 35 U.S.C. §112, second paragraph;
- E. Rejected claims 1-12 under 35 U.S.C. §112, second paragraph;
- F. Rejected claims 8-12 under 35 U.S.C. §112, second paragraph; and
- G. Rejected claims 1-12 35 U.S.C. §102(b) as allegedly being anticipated by U.S.

Patent No. 4,561,095 to Khan.

In this Response, Applicant respectfully traverses the foregoing objections and rejections and respectfully request allowance of all claims in view of the following amendments to the claims and the following remarks.

IN THE CLAIMS

Please amend claims 1-12 as follows:

Please substitute the following amended claim 1 for the currently pending claim 1.

1. (Amended) A test circuit for inclusion on an integrated circuit comprising:

a data unit identifier for identifying a data unit other than a next data unit to be transferred in a data unit sequence; and

an erroneous data verification parameter generator for generating an erroneous data verification parameter corresponding to said data unit identified by said data unit identifier, said corresponding erroneous data verification parameter signifying non-verification of data content of said identified data unit.

a¹ [Please substitute the following amended claim 2 for the currently pending claim 2.]

2. (Amended) The test circuit of claim 1, wherein said erroneous data verification parameter generator inverts a data verification parameter generated from said data content of said selected data unit.

[Please substitute the following amended claim 3 for the currently pending claim 3.]

3. (Amended) The test circuit of claim 1, wherein said erroneous data verification parameter generator inverts a portion of said data content of said selected data unit that is used to generate a data verification parameter.

[Please substitute the following amended claim 4 for the currently pending claim 4]

4. (Amended) The test circuit of claim 1, wherein said data unit identifier identifies a data group and said erroneous data verification parameter corresponds to said identified data group.

[Please substitute the following amended claim 5 for the currently pending claim 5]

5. (Amended) The test circuit of claim 1, wherein said data unit identifier uses data unit content to identify said data unit.

a! [Please substitute the following amended claim 6 for the currently pending claim 6]

6. (Amended) The test circuit of claim 1, wherein said data unit identifier uses data unit position to identify said data unit.

[Please substitute the following amended claim 7 for the currently pending claim 7]

7. (Amended) A method for real-time testing of a data receiver with data transmitted from an integrated circuit comprising:

identifying a data unit other than a next data unit to be transferred in a data sequence;
and
generating an erroneous data verification parameter signifying non-verification of data content of said identified data unit.

a! [Please substitute the following amended claim 8 for the currently pending claim 8.]

8. (Amended) The method of claim 7, wherein said generation of said erroneous data verification parameter includes inversion of a data verification parameter generated from said data content of said selected data unit.

[Please substitute the following amended claim 9 for the currently pending claim 9.]

9. (Amended) The method of claim 7, wherein said generation of said erroneous data verification parameter includes inversion of a portion of said data content of said selected data unit that is used to generate a data verification parameter.

[Please substitute the following amended claim 10 for the currently pending claim 10.]

10. (Amended) The method of claim 7, wherein said identification identifies a data group and said generated erroneous data verification parameter corresponds to said identified data group.

[Please substitute the following amended claim 11 for the currently pending claim 11]

11. (Amended) The method of claim 7, wherein said identification identifies a data unit using data unit content of said data unit.

a1 [Please substitute the following amended claim 12 for the currently pending claim 12]

12. (Amended) The method of claim 7, wherein said identification identifies a data unit using position of said data unit in a data sequence.

A marked-up version of each amended claim, showing the changes made thereto, is presented in Attachment II.

I. The Present Invention

The present invention is test circuitry and a method for real-time testing of data exception software that may be included on an integrated circuit. The circuitry supports the identification of a data unit or data group, other than a next data unit or group, to be transferred in a data sequence, and the generation of an erroneous data verification parameter that signifies non-verification of the data content of the identified data unit or group. The

identified data unit or group is later transmitted with the erroneous data verification parameter in real-time following transmission of other data units and/or groups having valid data verification parameters. In this manner, a data receiver may be tested to verify the detection of a data content error in real-time, and the execution of the software or firmware for processing an exception may be verified.

Test circuitry to implement the method of the present invention includes a data unit identifier for identifying a data unit or group within an integrated circuit, and an erroneous data verification parameter generator for generating an erroneous data verification parameter that is provided for storage or transfer with the identified data unit or group. The erroneous data verification parameter signifies non-verification of the data content of the identified data unit or group.

II. The Objection to the Drawings Should be Withdrawn

In the Office Action dated December 30, 2002, the Examiner objected to the drawings because the handwriting thereof was difficult to read. Applicant submits as Attachment I, four (4) sheets of corrected, informal drawings (Figs. 1, 1a, 2 and 3). It is respectfully submitted that these corrected drawings obviate the Examiner's objection. Applicant thus respectfully requests acceptance of the corrected drawings as a substitution for the drawings currently of record, and a withdrawal of the objection to the drawings.

III. The Objection to Claims 5 and 11 Should be Withdrawn

In the Office Action dated December 30, 2002, the Examiner objected to claims 5 and 11 because of informalities. Particularly, claims 5 and 11 were objected to with respect to the limitation of "data content" in lines 1-2 of each of claims 5 and 11, as improperly related back to "data content" of independent claims 1 and 7, from which claims 5 and 11 respectively depend. In response, Applicant has amended claims 5 and 11, to change "data content" to "data unit content".

In view of the above amendments to claims 5 and 11, Applicant respectfully requests withdrawal of the objection to claims 5 and 11.

IV. The §112, First Paragraph, Rejection of Claims 1-12 Should be Withdrawn

In the Office Action dated December 30, 2002, the Examiner rejected claims 1-12 under §112, first paragraph, as allegedly containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicant respectfully disagrees.

The Examiner indicates that "the Applicant teaches that the erroneous data verification parameter is used to verify the operation of the *data verification circuitry* (emphases added) and hence the data verification circuitry must carry out the operation of using the erroneous data verification parameter to verify data content of said identified data unit" (See 12/30/02 Office Action, page 3, heading #3). The Examiner then cites a limitation in independent claim

1 (and refers to a similar limitation in independent claim 7) that is indicated as rendering the claims non-enabling.

Applicant respectfully submits that the Examiner may be wrongly interpreting the present specification/invention. The erroneous data verification parameter, generated by the erroneous data verification generator, does not verify the operation of any "data verification circuitry." The erroneous data verification parameter is sent to the output register to be read along with the n-bit word stored therein. The erroneous data verification parameter indicates that the word (data) is not verified (non-verified) or is bad. This allows testing as presented in the summary of the Applicant's invention above (i.e. the artificial labeling of a data word as "bad"). Any "data verification circuitry" of the present invention is only for generating an erroneous data verification parameter for artificially marking a data unit as in error.

In view of the above, Applicant respectfully submits that claims 1-12 are enabling. Withdrawal of the §112, first paragraph, rejection is thus requested.

V. The §112, Second Paragraph, Rejection of Claims 1-6 and 8-12 Should be Withdrawn

In the Office Action dated December 30, 2002, the Examiner rejected claims 1-6 and 8-12 under §112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter with applicant regards as the invention. In view of the amendments to claims 1-6 and 7-12, Applicant respectfully disagrees.

Initially, it should be pointed out that claims 8-12 are method claims that depend from independent claim 7, and have been amended appropriately. Claims 1-6 are apparatus claims.

The term "data verification parameter generator" in independent claim 1 has been changed to "erroneous data verification parameter generator." The limitation of an erroneous data verification generator to indicate a circuit for producing an erroneous data verification parameter now renders claims 1-6 enabled. Since the erroneous data verification generator produces an erroneous data verification parameter, Applicant submits that claims 1-6 are enabled. Moreover, since claims 8-12 depend from claim 7, Applicant submits that claims 8-12 are enabled though independent claim 7.

In view of the above, Applicant respectfully requests withdrawal of the rejection to claims 1-6 and 8-12.

VI. The §112, Second Paragraph, Rejection of Claims 1-12 Should be Withdrawn

In the Office Action dated December 30, 2002, the Examiner rejected claims 1-12 under §112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter with applicant regards as the invention. In view of the amendments to claims 1-12, Applicant respectfully disagrees.

Particularly, the claims have been amended to recited that the erroneous data verification parameter signifies the non-verification of the data content of the identified data unit (with respect to independent claim 1), and signifying non-verification of data content of the identified data unit (with respect to independent claim 7). Therefore, it is now clear that the erroneous data verification parameter does not verify data content, but is used to signify the non-verification of data content, when the erroneous data verification parameter and the n-bit word are tested.

In view of the above, Applicant respectfully requests withdrawal of the rejection to claims 1-12.

VII. The §112, Second Paragraph, Rejection of Claims 8-12 Should be Withdrawn

In the Office Action dated December 30, 2002, the Examiner rejected claims 8-12 under §112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter with applicant regards as the invention, particularly with respect to the recitation of "The method." As pointed out above, claims 8-12 were intended and are now, in view of the amendments to claims 8-12, dependent upon the independent method claim 7.

Therefore, in view of the above, Applicant respectfully requests withdrawal of the rejection to claims 8-12.

VIII. The Prior Art Rejection of Claims 1-12 Should be Withdrawn

In the Office Action dated December 30, 2002, the Examiner rejected claims 1-12 under 35 U.S.C. Section 102(b) as allegedly being anticipated by U.S. Patent No. 4,561,095 to Khan (hereinafter, "Khan").

A. Khan

Khan is directed to a high speed error correcting random access memory system that includes a circuit for generation of a plurality of parity bits from a predetermined combination of data bits of a data word being stored in a random access memory such that these parity bits

are stored in memory along with the data bits, and for outputting the data work from the memory system. Khan also corrects for any single bit error in a data word by a circuit that generates a check work from the data work bits and parity word bits stored in the memory, whose state indicates if any of the data bits are in error, and if so, proceeds to correct any such erroneous bits.

B. The Claims

1. Claim 1

Applicant's claim 1, as amended, recites:

A test circuit for inclusion on an integrated circuit comprising:
a data unit identifier for identifying a data unit other than a next data unit to be transferred in a data unit sequence; and
an erroneous data verification parameter generator for generating an erroneous data verification parameter corresponding to said data unit identified by said data unit identifier, said corresponding erroneous data verification parameter signifying non-verification of data content of said identified data unit.

Independent claim 1 requires, among other limitations, requires the generation of an erroneous data verification parameter, with the erroneous data verification parameter signifying non-verification of data content of an identified data unit. This non-verification parameter is used for *testing* data communication circuitry, particularly of an IC. By artificially indicating that a word is erroneous, the circuitry can be checked. In contrast, Khan generates a plurality of parity bits from a predetermined combination of data bits of a data word being stored in the memory. These data bits are stored along with the word. When the word is output, any bits are corrected by the use of the stored parity bits. Khan thus does not generate an erroneous data verification parameter as defined in the present specification. Khan does not artificially

inject an error signal for test purposes as presently claimed.

In order for there to be anticipation of a claim under §102, each and every limitation must be taught in the cited reference. While Khan generates parity bits for correcting a word stored in memory, Khan does not artificially create an erroneous verification signal for testing the circuitry. Kahn is concerned with correcting erroneous bits/words.

In view of the above, it is respectfully submitted that Khan does not anticipate claim 1, since Khan does not teach each and every limitation of claim 1. Therefore, withdrawal of the rejection to and reconsideration of claim 1 is respectfully requested.

Claims 2-6

Each of claims 2-6 include independent claim 1 as a base claim. The reasoning set forth above with regard to the patentability of independent claim 1 is thus applicable to the patentability of claims 2-6, and is therefore incorporated herein by reference. As a result, each of claims 2-6 are not anticipated by Khan for the reasons hereinbefore discussed with regard to claim 1.

Further, each of the claims 2-6 includes further limitations that are not taught in Khan. Accordingly, reconsideration of claims 2-6 including withdrawal of the rejection thereto and allowance thereof is hereby respectfully requested.

2. Claim 7

Applicant's claim 7, as amended, recites:

A method for real-time testing of a data receiver with data transmitted from an integrated circuit comprising:

identifying a data unit other than a next data unit to be transferred in a data sequence; and

generating an erroneous data verification parameter signifying non-verification of data content of said identified data unit.

Independent claim 7 is directed to a method for real-time testing of a data receiver with data transmitted from an integrated circuit having similar limitations to independent claim 1.

As such, the arguments with respect to independent claim 1 are applicable to claim 7 and are hereby incorporated herein. It has been shown above, that independent claim 1 is not anticipated by Khan. Therefore, claim 7 cannot be anticipated by Khan for the same reasoning.

In view of the above, it is respectfully submitted that Khan does not anticipate claim 7, since Khan does not teach each and every limitation of claim 7. Therefore, withdrawal of the rejection to and reconsideration of claim 7 is respectfully requested.

Claims 8-12

Each of claims 8-12 include independent claim 7 as a base claim. The reasoning set forth above with regard to the patentability of independent claim 7 is thus applicable to the patentability of claims 8-12, and is therefore incorporated herein by reference. As a result, each of claims 8-12 are not anticipated by Khan for the reasons hereinbefore discussed with regard to claim 7.

Further, each of the claims 8-12 includes further limitations that are not taught in Khan. Accordingly, reconsideration of claims 8-12 including withdrawal of the rejection thereto and allowance thereof is hereby respectfully requested.

IX. Conclusion

It is respectfully submitted that all claims are in condition for allowance. Accordingly, withdrawal of all objections and rejections, reconsideration, and prompt and favorable examination is earnestly solicited for all claims.

Respectfully Submitted,

A handwritten signature in black ink, appearing to read "Bruce J. Bowman", with a large, stylized initial "B" and "J".

April 30, 2003

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ATTACHMENT II

Marked-up Version of Amended Claims 1-12 Showing Changes Made Thereto

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1. (Amended) A test circuit for inclusion on an integrated circuit comprising:

a data unit identifier for identifying a data unit other than a next data unit to be transferred in a data unit sequence; and

[a] an erroneous data verification parameter generator for generating an erroneous data verification parameter corresponding to said data unit identified by said data unit identifier, [so that] said corresponding erroneous data verification parameter [does not verify] signifying non-verification of data content of said identified data unit.

2. (Amended) The test circuit of claim 1, wherein said erroneous data verification parameter generator inverts a data verification parameter generated from said data content of said selected data unit.

3. (Amended) The test circuit of claim 1, wherein said erroneous data verification parameter generator inverts a portion of said data content of said selected data unit that is used to generate a data verification parameter.

4. (Amended) The test circuit of claim 1, wherein said data unit identifier identifies a data group and said erroneous data verification parameter corresponds to said identified data group.

5. (Amended) The test circuit of claim 1, wherein said data unit identifier uses data unit content to identify said data unit.

6. (Amended) The test circuit of claim 1, wherein said data unit identifier uses data unit position to identify said data unit.

7. (Amended) A method for real-time testing of a data receiver with data transmitted from an integrated circuit comprising:

identifying a data unit other than a next data unit to be transferred in a data sequence;
and

generating an erroneous data verification parameter [that does not verify] signifying non-verification of data content of said identified data unit.

8. (Amended) The method of claim [5] 7, wherein said generation of said erroneous data verification parameter includes inversion of a data verification parameter generated from said data content of said selected data unit.

9. (Amended) The method of claim [5] 7, wherein said generation of said erroneous data verification parameter includes inversion of a portion of said data content of said selected data unit that is used to generate a data verification parameter.

10. (Amended) The method of claim [5] 7, wherein said identification identifies a data group and said generated erroneous data verification parameter corresponds to said identified data group.

11. (Amended) The method of claim [5] 7, wherein said identification identifies a data unit using data unit content of said data unit.

12. (Amended) The method of claim [5] 7, wherein said identification identifies a data unit using position of said data unit in a data sequence.